Design and Simulation of FPGA-based Serial Data Control for a Readout Control in a Calorimeter

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ABSTRACT

The readout control of the calorimeter of former ZEUS detector uses serial data input to preset the controlling bits in the RAM unit of the table control sub-module of the readout control. Programmable Gate Array (FPGA) was used to configure a table control sub-module of the readout control using hardware descriptive language (HDL) Verilog. In this paper, the configuration and simulation result serial data in the FPGA-based table control is described.

ABSTRAK

Sistem kawalan 'readout' di calorimeter pengesan ZEUS menggunakan data masukan siri yang diguna untuk preset bit-bit kawalan dalam unit RAM di dalam modul kawalan 'table' sebagai sub-modul system kawalan 'readout'. Programmable Gate Array (FPGA) telah digunakan untuk membina susunatur modul kawalan 'table' dengan menggunakan bahasa huraian peranti (HDL) Verilog. Dalam kertas ini, susunatur dan hasil simulasi data siri dalam modul kawalan 'table' berasaskan FPGA dihuraikan. .

Keywords: readout control, RAM, serial data

INTRODUCTION

In the former ZEUS detector at HERA (Hadron-Electron Ring Accelerator), the data taking in the high energy physics experiments from the electron-proton collision that moved the speed of 30GeV and 920 GeV respectively, were collected using five readout analog controlling modules i.e. the table, pipeline, buffer, format and generator, with more than 140 signals interconnected to each other within the main module. These data were recorded by ZEUS detector, synchronized by the HERA clock at 96 ns or 10MHz. In the table module, serial data that consist of 4 byte of data in the random access memory (RAM), preset the controlling bits of the readout system. In this paper, the Programmable Gate Array (FPGA) based table is described using a 24-bits serial data for online control is described.

THE TABLE CONTROL MODULE

Figure 1 gives the readout control of the calorimeter in the ZEUS detector, showing five controlling modules i.e. table, pipeline, buffer, format and generator. The function of each modules were as follows: the pipeline module selected which particular cell out of 96 samples to trigger [2] during the data taking of the physics experiment; the buffer kept the interim data storage received from the pipeline; the table module interfaced between the global first level trigger (GFLT) and the calorimeter readout electronics; the format controller controlled the timing for the digitization of the output; the pulse generator controlled test pulses during data taking and during various offline operation.

In offline mode, the 16-bits serial data was send to the RAM unit in the table module to set the controlling bits on sample delay, number of sample, event types, output format, event type, online/offline and synchronization of the data taking during the physics experiment, the bits were counted by a 2MHz serial clock.

The controlling data during online operation of the readout system was kept in the RAM of the table module. During offline operation, a 16-bits serial data synchronized by a 10MHz clock asynchronized to HERA clock was send the RAM via a 16-bits shift register. The first bit of the serial data would be pushed up to the 16^{th} bit in the RAM. This process continued until the 16^{th} bit of the serial data was in the register, before the system was set online for the GFLT trigger synchronized by the 96 ns HERA clock. The controlling data included delay time to complete each set of data taking out of 96 samples, the number of samples, the type of and events being triggered. Figure 2 gives the serial input block diagram in the table module of the readout controller [1], [4].

FPGA Based serial data control was designed with Verilog using 16-bit shift register to accept serial data and serial clock and compared them with the GFLT signals. The readout control system was first isolated by giving flag 0, before each subsequent byte pushed the prior byte onto the next register in the chain [1]. Once set, the readout control was put on-line again, where the signals from GFLT (Global First Level Trigger) would determine the controlling sequence of the readout control.

SERIAL DATA SIMULATION AND RESULTS

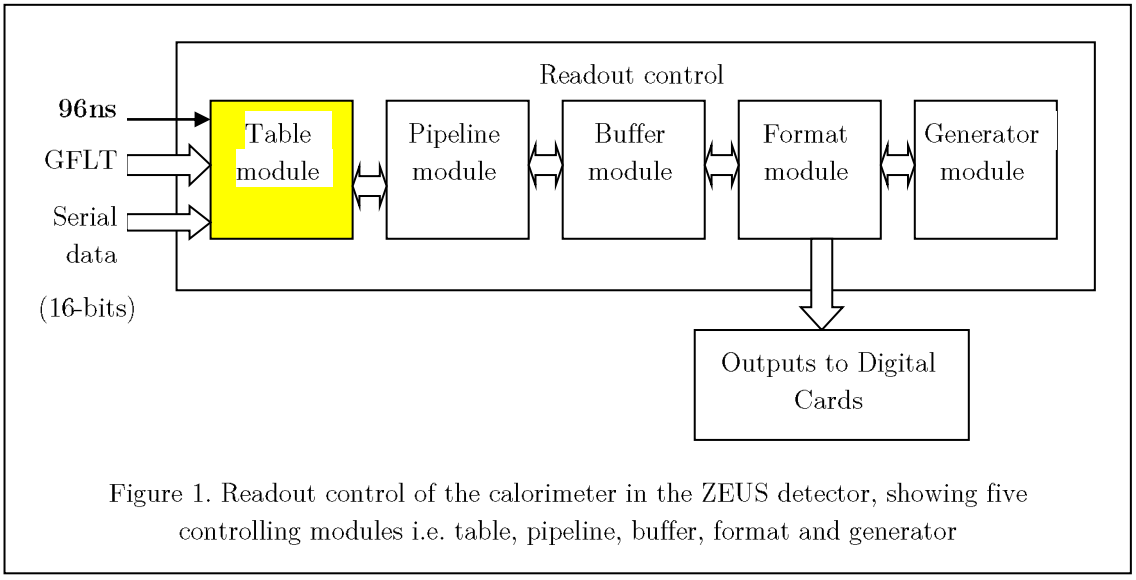
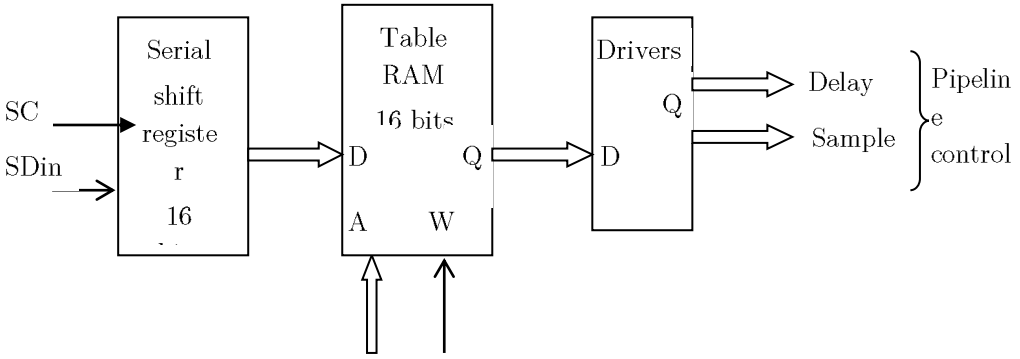


Figure 1. Readout control of the calorimeter in the ZEUS detector, showing five controlling modules i.e. table, pipeline, buffer, format and generator



Legend:SC- Serial Clock; SDin - Serial Data input; A - GFLT Trigger; WE- Write

Figure 2. Serial input block diagram in the table module of the readout controller

In Figure 3, the RAM block in the table module of the FPGA-based readout controller is given, while Table 1 gives the input/output label from FPGA-based readout control (ROC) and their status. **Figure 4** shows part of the vector waveform used in Quartus II for the simulation for serial data input. Each serial data consist of 4 bytes control data given to RAM in table module. Each bit of the serial data is only counted on negative change of the clock edge, where subsequent byte pushes a prior byte up the 16-bit shift register.

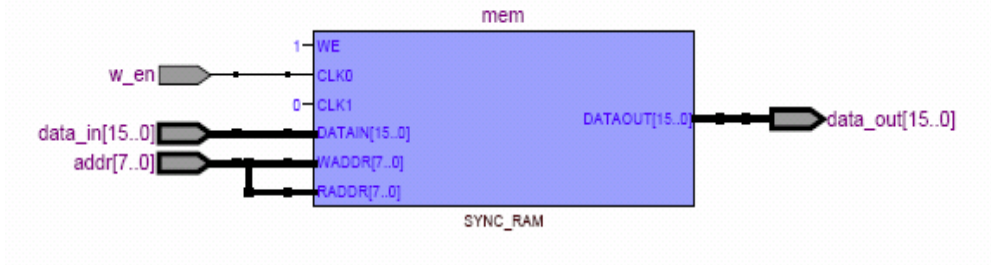


Figure 3. The RAM block in the table module of the FPGA-based readout controller

Figure 4 shows the 16-bits serial data vector waveform inputs on Quartus II, of the table, pipeline, format, buffer and generator during an offline operation and synchronized by a 10MHz clock. Each bit of the serial data is only counted on negative change of the clock edge, where subsequent byte pushes a prior byte up the 16-bit shift register [3].

During an online operation, the readout controller would be hooked to the GFLT signals. The trigger signals from the GFLT would be compared against the preset values in the RAM. The buffer controller would continue taking the physics data event and forward them to format controller for digital outputs for as long as the accept (ACT) signal from the GFLT is true. When the abort (ABT) flag 1 from the GFLT is received by the buffer controller via the pipeline controller, the buffer controller would abort the current data transfer and start a new data transfer once the pipeline accept (PACT) flag 1 was received from the pipeline controller.

Table 1 . Some of the input/output label from FPGA-based readout control (ROC) and their status

Input label	**Input Status**	**Flag**	**Ouput label**	**Output Status**	**Flag**
HERA clock (CP)	96ns	clock	GFLT_busy	GFLT busy	1
Global First Level Trigger (GFLT)	GFLT[12] Accept (ACT)	**1**	Offline	System is off-line	1
	GFLT[11] Abort (ABT)	**1**	STRB	Strobe signal	0
Serial [7:0]			TYP	Type of event	000
Serial [1]	Table	16 bits	TSTEN	Test mode enable	0
Serial [3]	Pipeline	16 bits	DBSY	Data busy	0

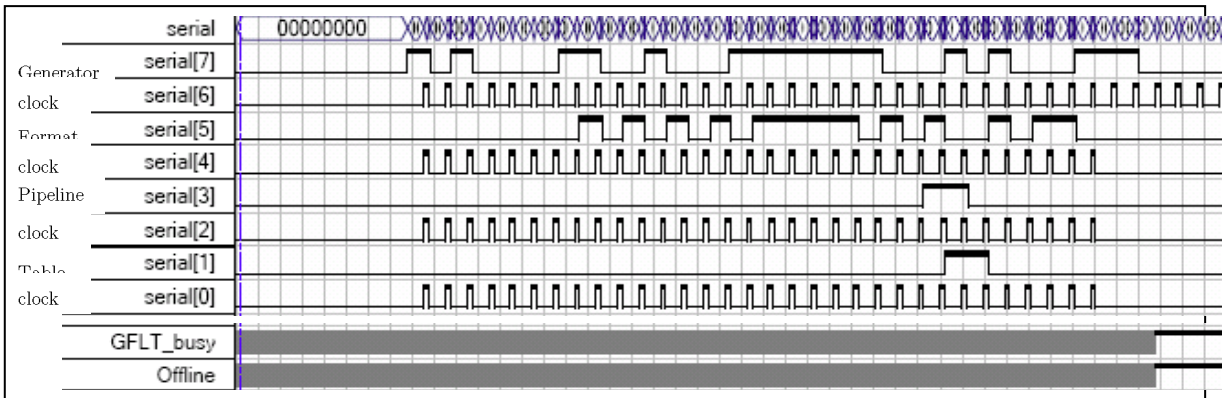


Figure 4. Simulation wave form of 16-bits serial input data for readout control, during offline, with negative edge clock trigger on Quartus II

Figure 5 gives part of the vector waveform output signals of FPGA-based readout control simulated on Quartus II using the device settings of Altera Cylcone and synchronized by a 96 ns global clock. From this figure, it could be seen that while the GFLT [12] flag is 1, the accept flags in both the pipeline (PACT) and buffer (BACT) remain 1. On receiving the abort flag 1 from the GFLT [11], the pipeline abort (PABT) flag is also 1.

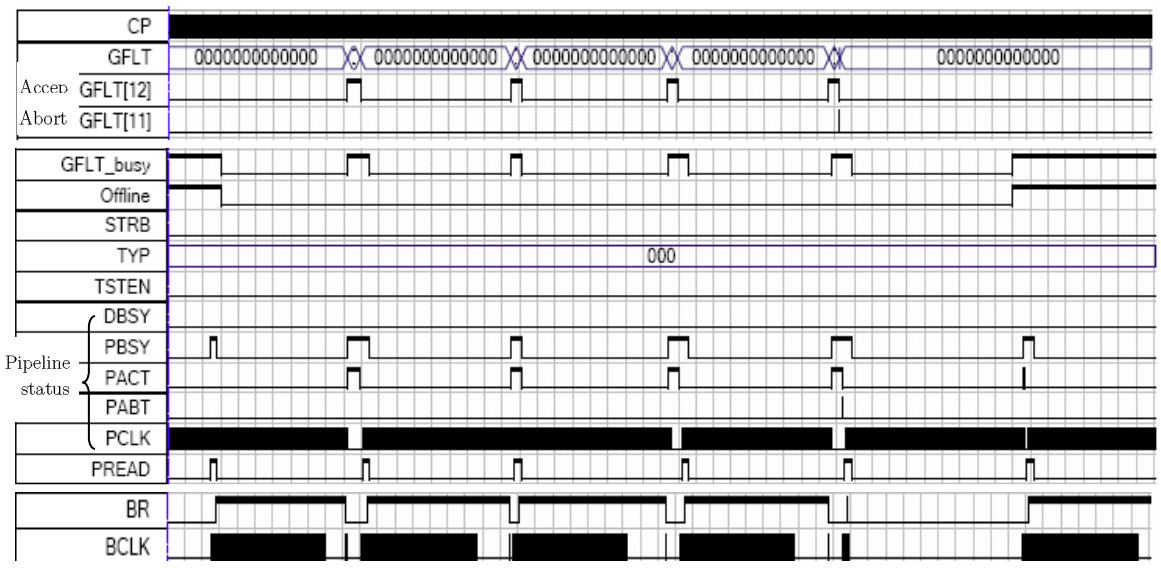


Figure 5. Simulation wave form of output from FPGA-based readout control, during online

CONCLUSIONS

The used of FPGA-based RAM in a 16-bit serial data control of a readout system in the ZEUS calorimeter provided a very useful and convenient method for serial data control analysis. It is compact and easier to modify, than the conventional analog system.

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